

In the Specification:

Please replace the paragraph beginning on page 8, line 9 and ending on page 8, line 19 with the following amended paragraph:

As shown in Figure 1, cascode amplifier circuit 102 comprises FETs 104, 106, 108, and 110, where the source of FET 104 at node 120 is connected to the drain of target memory cell 112, typically by a selection circuit (not shown), through bit line 116 during a read operation involving target memory cell 112. During the read operation, the source of target memory cell 112 is also connected to a reference voltage, such as ground 130, and the gate of target memory cell 112 is selected to turn on target memory cell 112, which draws I_{core} 118 via bit line 116. PFET 124 and PFET 126 operate as enable transistors to switch on cascode amplifier circuit 102 during a read operation involving target memory cell 112. More specifically, PFET 124 is enabled to connect supply voltage ("VCC") 128 to the drain of ~~PFET~~ FET 108, PFET 126 is enabled to connect VCC 128 to the drain of PFET 110.

Please replace the paragraph beginning on page 9, line 12 and ending on page 10, line 14 with the following amended paragraph:

In cascode amplifier circuit 102, FET 104 operates as a primary cascode transistor, FETs 106 and 110 operate as a negative feedback to FET 104 for stabilizing DATAB 120, and FET 108 operates as a load ~~a load~~ across VCC 128 and the drain of FET 104. With this arrangement, cascode amplifier circuit 102 generates DATAB 120, which has a lower operating bound and a wider range to accommodate numerous memory cell types. For example, with reference to

Attorney Docket No.: 0180185

Figure 2, graph 200 illustrates DATAB 120 and current 114 drawn by FET 106 as a function of DCNT 132 sweeping from 5V to 0V, as achieved by cascode amplifier circuit 102. In Figure 2, DATAB curve 202 corresponds to DATAB 120, current curve 204 corresponds to current 114 drawn by FET 106 when cascode amplifier circuit 102 is activated, and DCNT curve 206 corresponds to DCNT 132 supplied to the gate of FET 110. As shown in graph 200, when current curve 204 approaches the lower bound of approximately 4 micro Amps (μA) at point 208, cascode amplifier circuit 102 is operating and generates DATAB 120 of approximately 0.5V (corresponding to DATAB curve 202 at point 210). Thus, with DCNT 132 of approximately 2.5V (corresponding to DCNT curve 206 at point 212), cascode amplifier circuit 102 is operating, and DATAB 120 has a voltage of approximately 0.5V, which is suitable for use with target memory cell 112 capable of storing a single bit. Continuing with graph 200, with DCNT 132 of approximately 5V (corresponding to DCNT curve 206 at point 216), DATAB 120 has a voltage of approximately 1.5V (corresponding to DATAB curve 202 at point 214), which is suitable for use with target memory cell 112 capable of storing two binary bits. As illustrated by the above examples, due to the particular arrangement of cascode amplifier circuit 102, the flexible and wide voltage range for DATAB 120 achieved by cascode amplifier circuit 102 allows cascode amplifier circuit 102 to be used with a wide variety of memory cells.